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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,595	06/25/2003	Keisuke Yonehama	239515US2	1422
22850	7590	06/16/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			OWENS, DOUGLAS W	
		ART UNIT	PAPER NUMBER	
		2811		
DATE MAILED: 06/16/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/602,595	YONEHAMA ET AL.	
	Examiner	Art Unit	
	Douglas W. Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 May 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-17 and 19-30 is/are rejected.
- 7) Claim(s) 18 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 16, 2005 has been entered.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1 – 30 are objected to because of the following informalities: In line 1 of claim 1, --comprising--, --consisting of--, or a similar term should be inserted after “device”.

In line 2 of claims 3 and 6, --wherein-- should be inserted after “claim 1”.

In line 2 of claims 4 and 5, --wherein-- should be inserted after “clam 3”.

In line 12 of claim 16, “inter layer” should be replaced with --interlayer--.

In line 2 of claims 18 – 21, --wherein-- should be inserted after “claim 16,”

Appropriate correction is required.

Allowable Subject Matter

5. The indicated allowability of claims 16 – 30 is withdrawn in view of the newly discovered reference(s) to Hirai et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 6, 16, 17 and 19 – 21 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,703,676 to Hirai et al.

Regarding claim 1, Hirai et al. teach a semiconductor memory device (Figs. 18A and 18B), comprising:

a first memory cell (left side, for example) having a first gate electrode (4), a first diffusion layer (6) and a second diffusion layer (5), the first and second diffusion layers arranged in a substrate to be adjacent to the first gate electrode;

a first contact layer (9) connected to the first diffusion layer of the first memory cell;

a second contact layer (14, 19) electrically connected to the first contact layer;

a first bit line (21) connected to the second contact layer and arranged above the first gate electrode of the first memory cell;

a second memory cell (right side) having a second gate electrode (4), a third diffusion layer (6) and a fourth diffusion layer (5), the third and fourth diffusion layer arranged in a semiconductor substrate to be adjacent to the second gate electrode, the second gate electrode of the second memory cell electrically connected to the first gate electrode of the first memory cell, the first and second memory cells arranged in a direction perpendicular to the first bit line;

a second bit line (21; Fig. 18A) connected to the third diffusion layer, arranged above the second gate electrode of the second memory cell, and arranged parallel to the first bit line; and

a conductive layer (9) commonly connected to the second diffusion layer (5) of the first memory cell and the fourth diffusion layer of the second memory cell, a height

of the conductive layer substantially being coplanar with a height of the first contact layer.

Regarding claims 2 and 17, Hirai et al. teach a device, wherein the first contact layer includes a tungsten layer (Col. 5, lines 62 and 63).

Regarding claims 6 and 21, Hirai et al. teach a device, wherein the memory device is a nonvolatile device. The limitation of using the device in a NAND or NOR type memory is considered a suggested use limitation and is not given any patentable weight.

Regarding claim 16, Hirai et al. teach a semiconductor memory device, comprising:

- a plurality of memory cells, each of which includes a gate electrode (4) and a diffusion layer (6, 5);
- an insulting film (23) formed above side and top surfaces of each gate electrode of the plurality of memory cells;
- a first interlayer insulating layer (7) formed between two gate electrodes adjacent to each other;
- a first contact layer (9) formed in the first interlayer insulating layer and connected to the diffusion layer;
- a second interlayer insulating layer (11) formed on the first interlayer insulting layer;
- a second contact layer (14) formed in the second interlayer insulating layer and electrically connected to the first contact layer;

a bit line (21) electrically connected to the second contact layer; and
a conductive layer (9) connected to at least two of the diffusion layers (5) other
than the diffusion layer connected to the first contact layer, the conductive layer formed
between the two gate electrodes being arranged in a direction vertical to the bit line, a
height of the conductive layer substantially being coplanar with a height of the first
contact layer.

Regarding claim 19, Hirai et al. teach a device, wherein a position of a top
surface of the insulating film formed above the gate electrode of the plurality of memory
cells is different from that of the top surface of the first interlayer insulating layer.

Regarding claim 20, Hirai et al. teach a device, wherein the conductive layer is a
source line.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all
obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set
forth in section 102 of this title, if the differences between the subject matter sought to be patented and
the prior art are such that the subject matter as a whole would have been obvious at the time the
invention was made to a person having ordinary skill in the art to which said subject matter pertains.
Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over
Hirai et al. as applied to claim 1 above, and further in view of US Patent Application
Publication No. 2001/0008311 to Harada et al.

Hirai et al. teach a device, wherein the first contact layer includes a tungsten film.
Hirai et al. do not teach a device, wherein the first contact layer includes a first and
second conductive film, the first conductive film comprising titanium and the second

conductive film comprising tungsten. Harada et al. teach a semiconductor device (Fig. 2C), wherein the contact layer includes a first (12a) and second (12b) conductive film, wherein the first conductive film is titanium (paragraph [0096]) and the second film is tungsten. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Harada et al. into the device taught by Hirai et al., since it is desirable to prevent unwanted diffusion of tungsten, as well as provide an adhesion layer to prevent the tungsten from peeling.

10. Claims 7 – 15 and 22 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirai et al. as applied to claims 1 and 16 above, and further in view of US Patent No. 6,731,538 to Noda et al.

Regarding claims 7 and 22, Hirai et al. do not teach a memory card including the semiconductor memory device. Noda et al. teach a memory card (fig. 19) including a semiconductor memory device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching Noda et al. into the device taught by Hirai et al. since it is desirable to provide housing and connectability for memory devices.

Regarding claims 8 and 23, Hirai et al. do not teach a card holder to which the memory card is inserted. Noda et al. teach a card holder (Fig. 21) to which the memory card is inserted. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Noda et al. into the device taught by Hirai et al., since it is desirable to securely hold the device of the suggested modification in the discussion of claim 7 above.

Regarding claims 9, 10, 24 and 25 Hirai et al. do not teach a connecting device to which the memory card is inserted, wherein the connecting device is configured to be connected to a computer. Noda et al. teach a connecting device to which the memory card is inserted, wherein the connecting device is configured to be connected to a computer (Fig. 23). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Noda et al. into the device taught by Hirai et al., since it is desirable to enable communication between the modified device and external devices.

Regarding claims 11 and 26, Hirai et al. do not teach a memory card including the semiconductor memory device and a controller which controls the semiconductor memory device. Noda et al. teach a memory card including the semiconductor memory device and a controller which controls the semiconductor memory device (Fig. 20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Noda et al. into the device taught by Hirai et al. since it is desirable to provide memory for memory cards, as well as controlling said memory.

Regarding claims 12 and 27, Hirai et al. do not teach a card holder to which the memory card is inserted. Noda et al. teach a card holder (Fig. 21) to which the memory card is inserted. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Noda et al. into the teaching of Hirai et al., since it is desirable to securely hold the device of the suggested modification suggested in the discussion of claim 11 above.

Regarding claims 13, 14, 28 and 29 Hirai et al. do not teach a connecting device to which the memory card is inserted, wherein the connecting device is configured to be connected to a computer. Noda et al. teach a connecting device to which the memory card is inserted, wherein the connecting device is configured to be connected to a computer (Fig. 23). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Noda et al. into the teaching of Hirai et al., since it is desirable to enable communication between the modified device (discussed in the rejection of claim 11) and external devices.

Regarding claims 15 and 30, Hirai et al. do not teach an IC card including the semiconductor memory device. Noda et al. teach an IC card (Fig. 20) including a semiconductor memory device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Noda et al. into the device taught by Hirai et al. since it is desirable to provide memory for memory cards and IC cards.

Response to Arguments

11. Applicant's arguments with respect to claims 1 – 15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Douglas W Owens
Examiner
Art Unit 2811

DWO